

The diagram illustrates a pixel circuit (70) with the following components and connections:

- Vertical Selection Circuit (3):** Consists of two PMOS transistors (8-1, 8-2) and two NMOS transistors (5-1, 5-2). The gates of 8-1 and 8-2 are connected to V_s . The gates of 5-1 and 5-2 are connected to the output of the row selection circuit (40).
- Row Selection Circuit (40):** A vertical block that receives V_d, V_s and outputs V_1 and V_2 to the gates of transistors 5-1 and 5-2, respectively.
- Pixel Circuit (70):**
 - Contains two PMOS transistors (61, 62) and two NMOS transistors (10, 13).
 - The gates of 61 and 62 are connected to the output of the horizontal selection circuit (70).
 - The gates of 10 and 13 are connected to the output of the row selection circuit (40).
 - The sources of 61 and 62 are connected to V_{C1} and V_{C2} , respectively.
 - The sources of 10 and 13 are connected to V_{C1} and V_{C2} , respectively.
 - The drains of 10 and 13 are connected to V_{C1} and V_{C2} , respectively.
 - The drains of 61 and 62 are connected to V_{C1} and V_{C2} , respectively.
 - The drains of 10 and 13 are connected to V_{C1} and V_{C2} , respectively.
 - The drains of 61 and 62 are connected to V_{C1} and V_{C2} , respectively.
- Other Components:**
 - Capacitors 11 and 12 are connected between the gates of 5-1 and 5-2 and the gates of 61 and 62, respectively.
 - Capacitors 15 and 16 are connected between the gates of 8-1 and 8-2 and the gates of 61 and 62, respectively.
 - Capacitors 17 and 18 are connected between the gates of 5-1 and 5-2 and the gates of 10 and 13, respectively.
 - Capacitors 19 and 20 are connected between the gates of 61 and 62 and the gates of 10 and 13, respectively.
 - Capacitors 21 and 22 are connected between the gates of 10 and 13 and the gates of 61 and 62, respectively.
 - Capacitors 23 and 24 are connected between the gates of 61 and 62 and the gates of 10 and 13, respectively.

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FIG. 2A

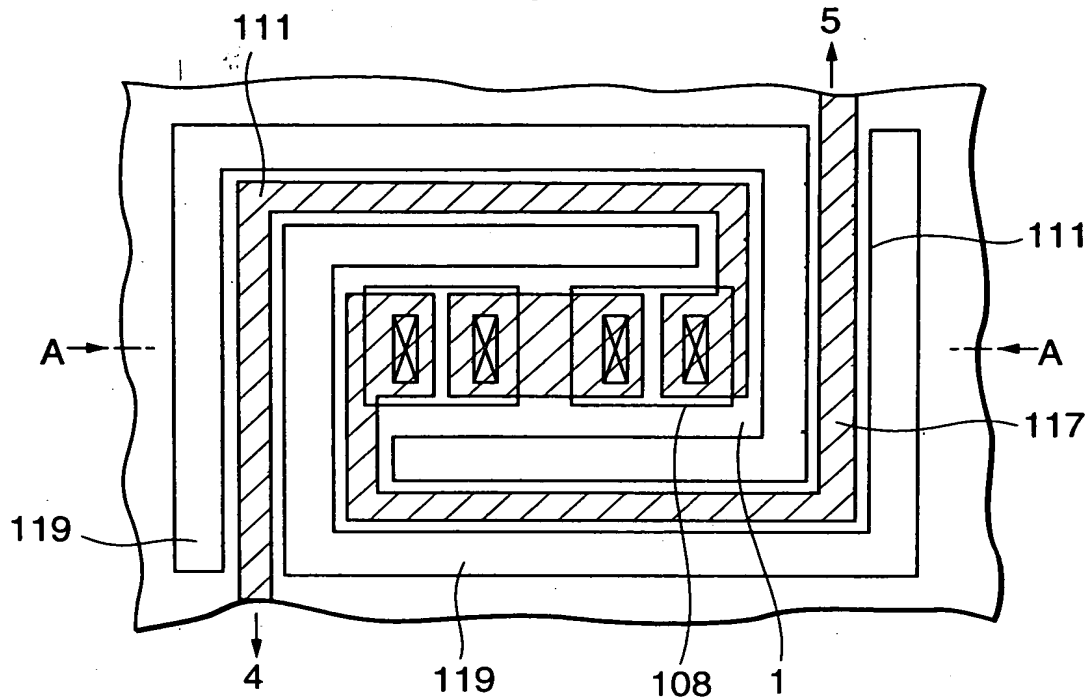
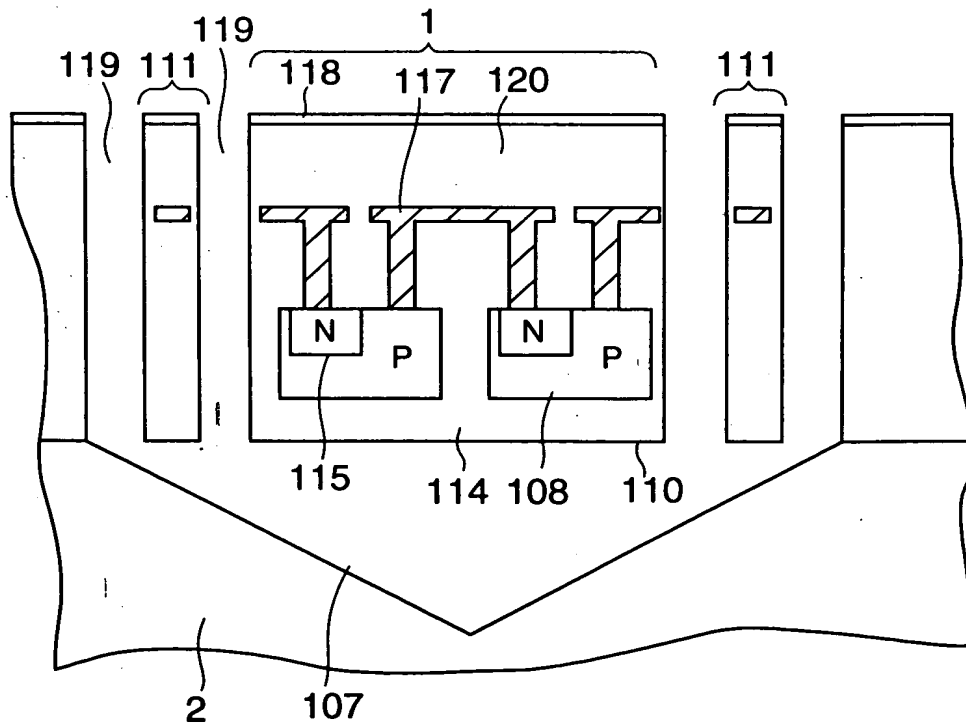
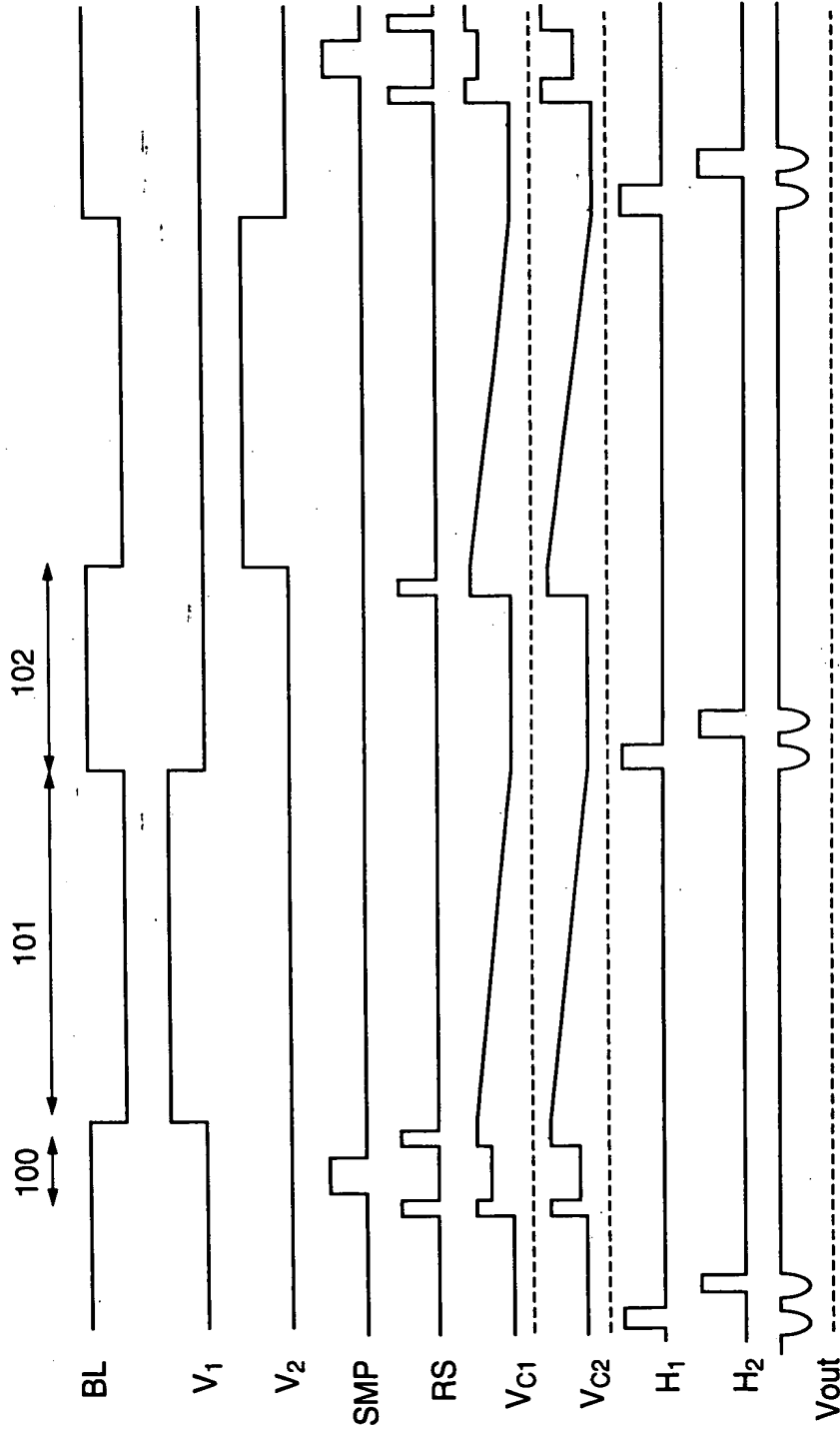


FIG. 2B



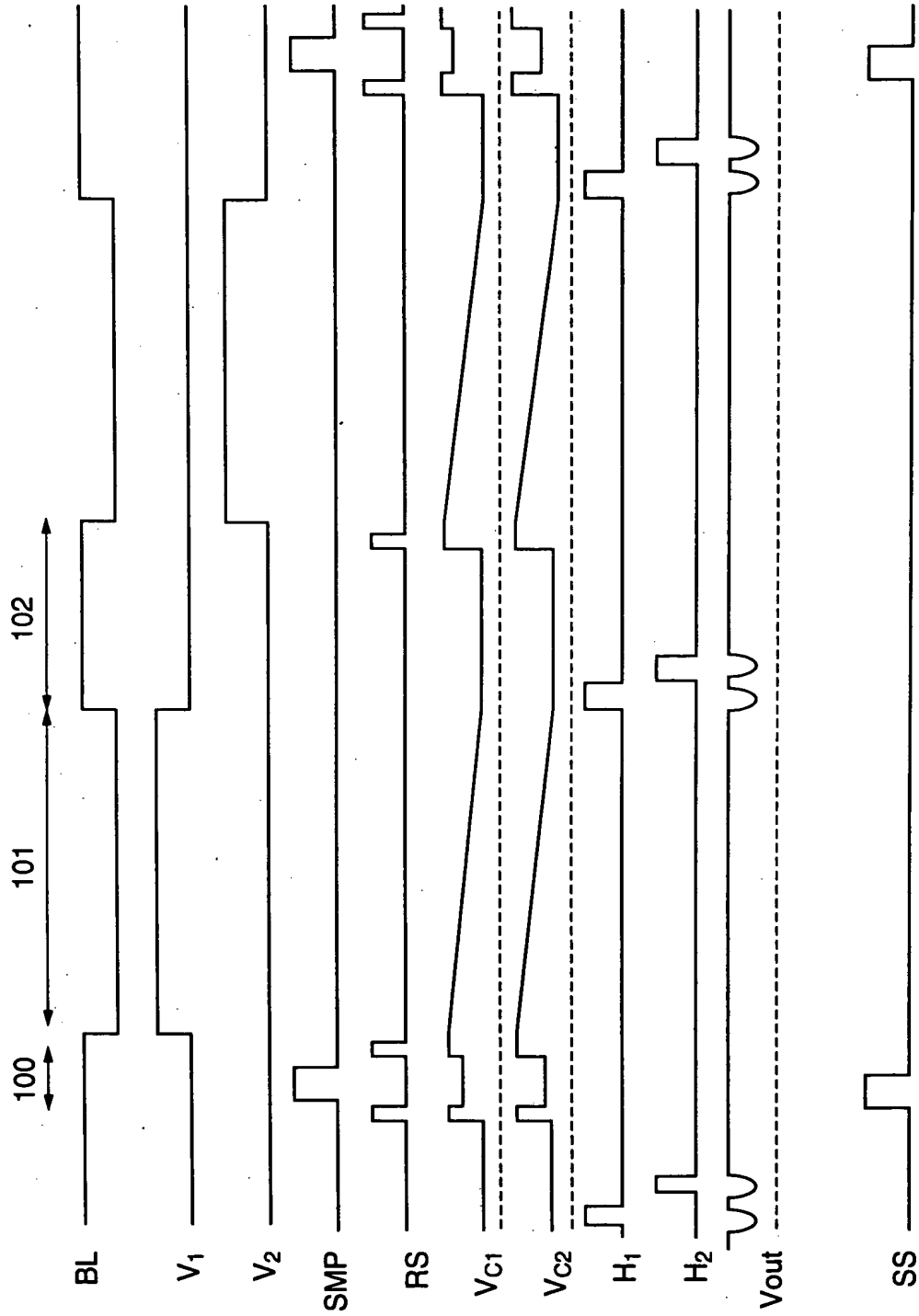
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FIG. 3



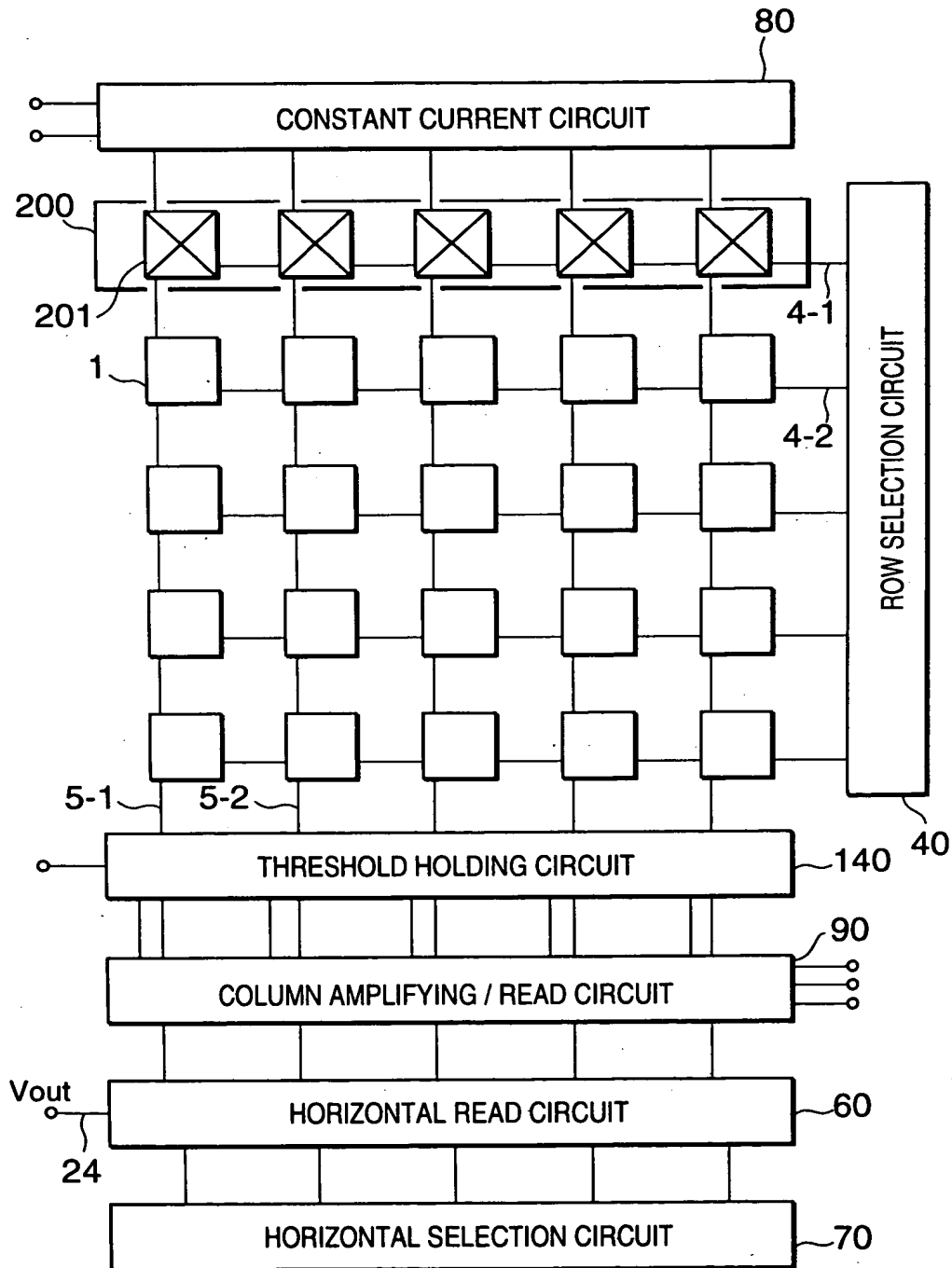
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FIG. 4



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FIG. 5



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FIG. 6A

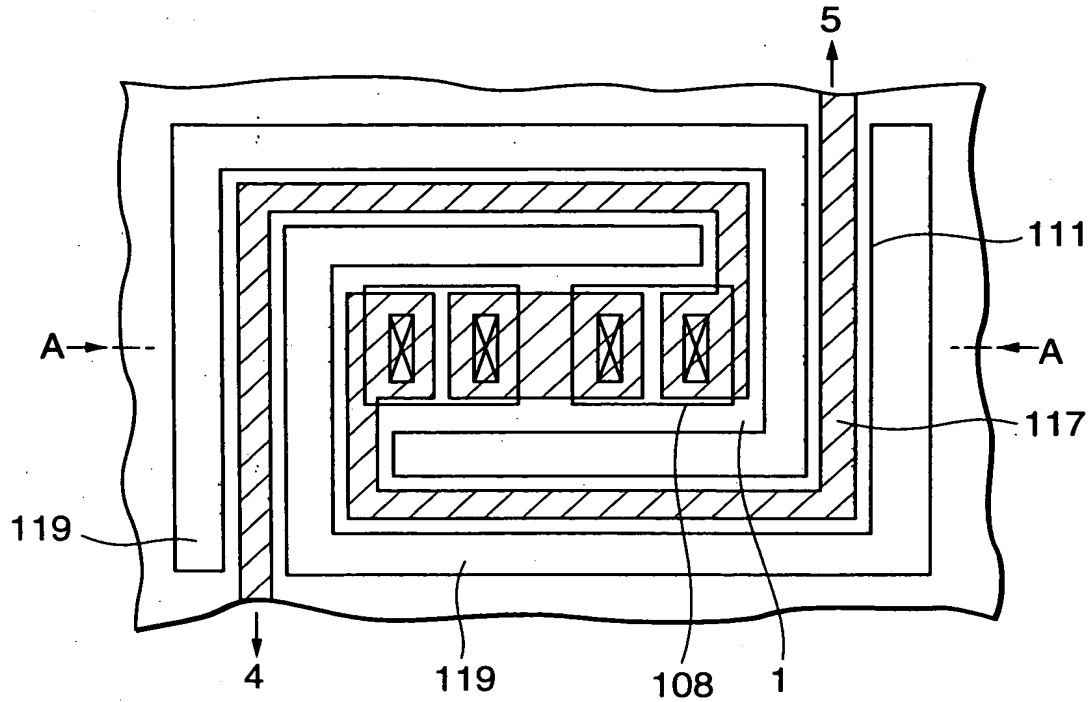
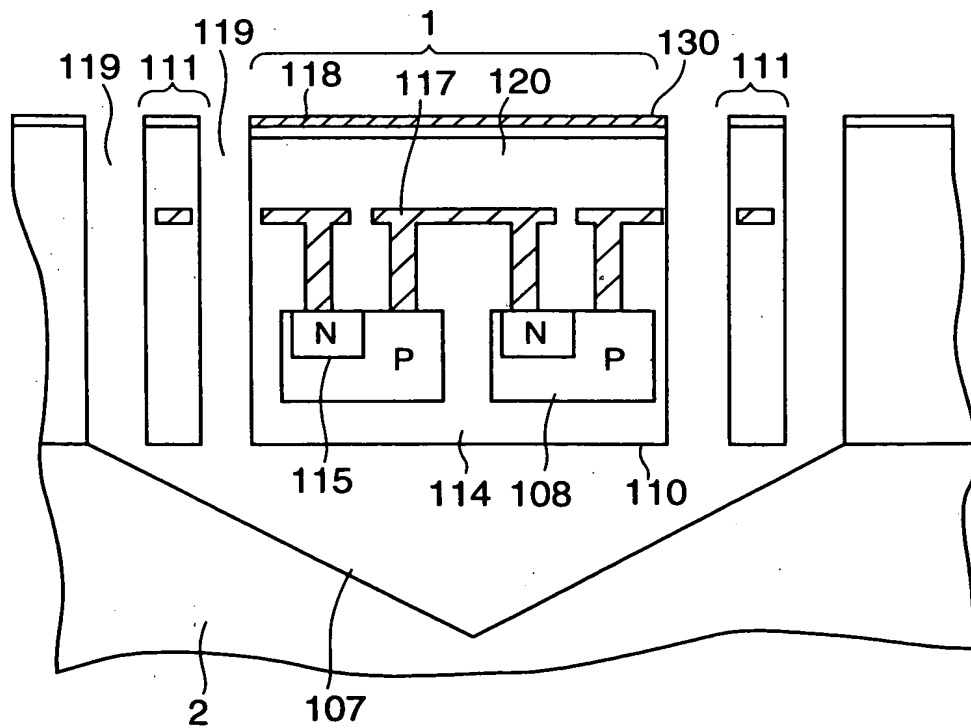
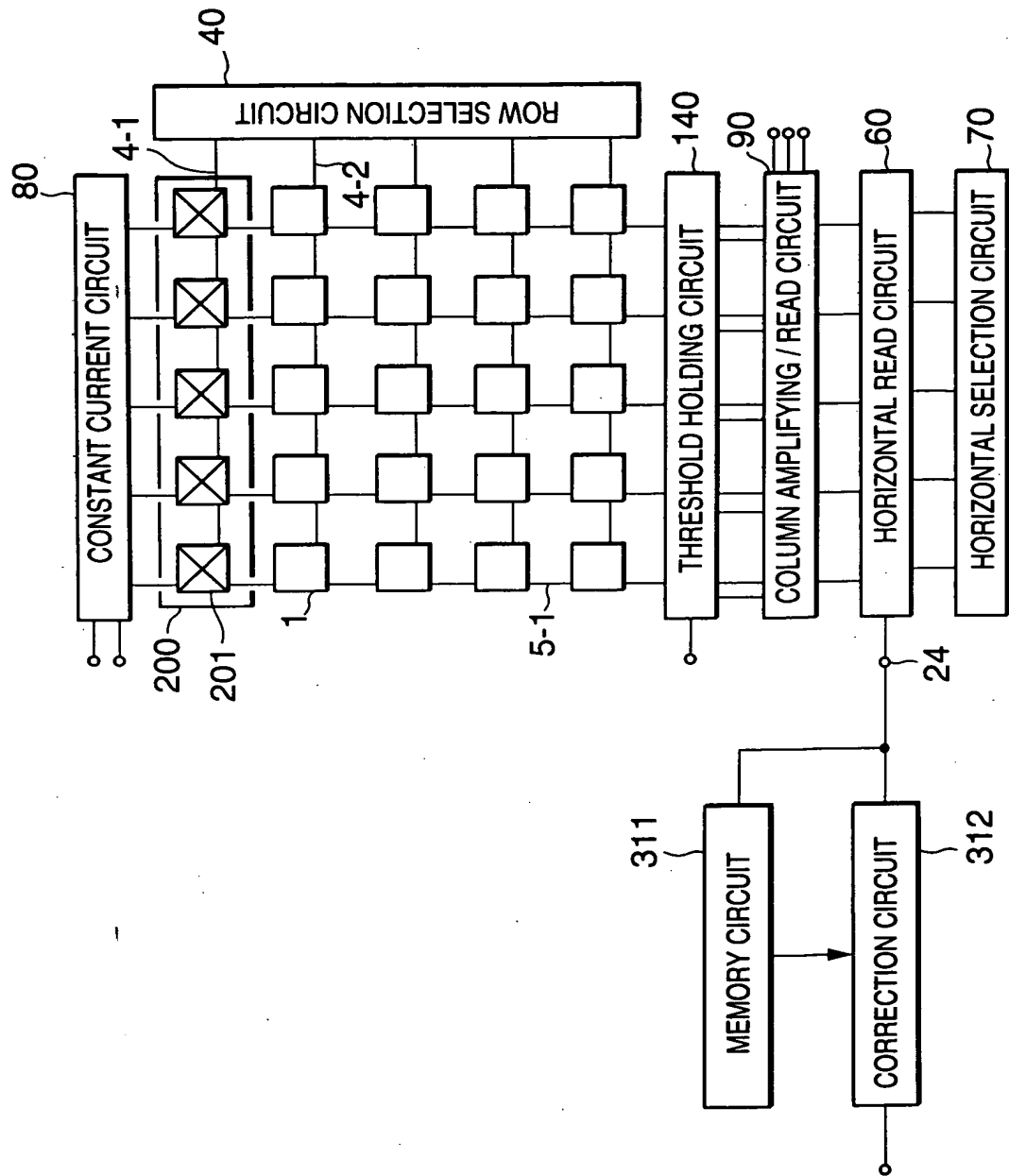


FIG. 6B



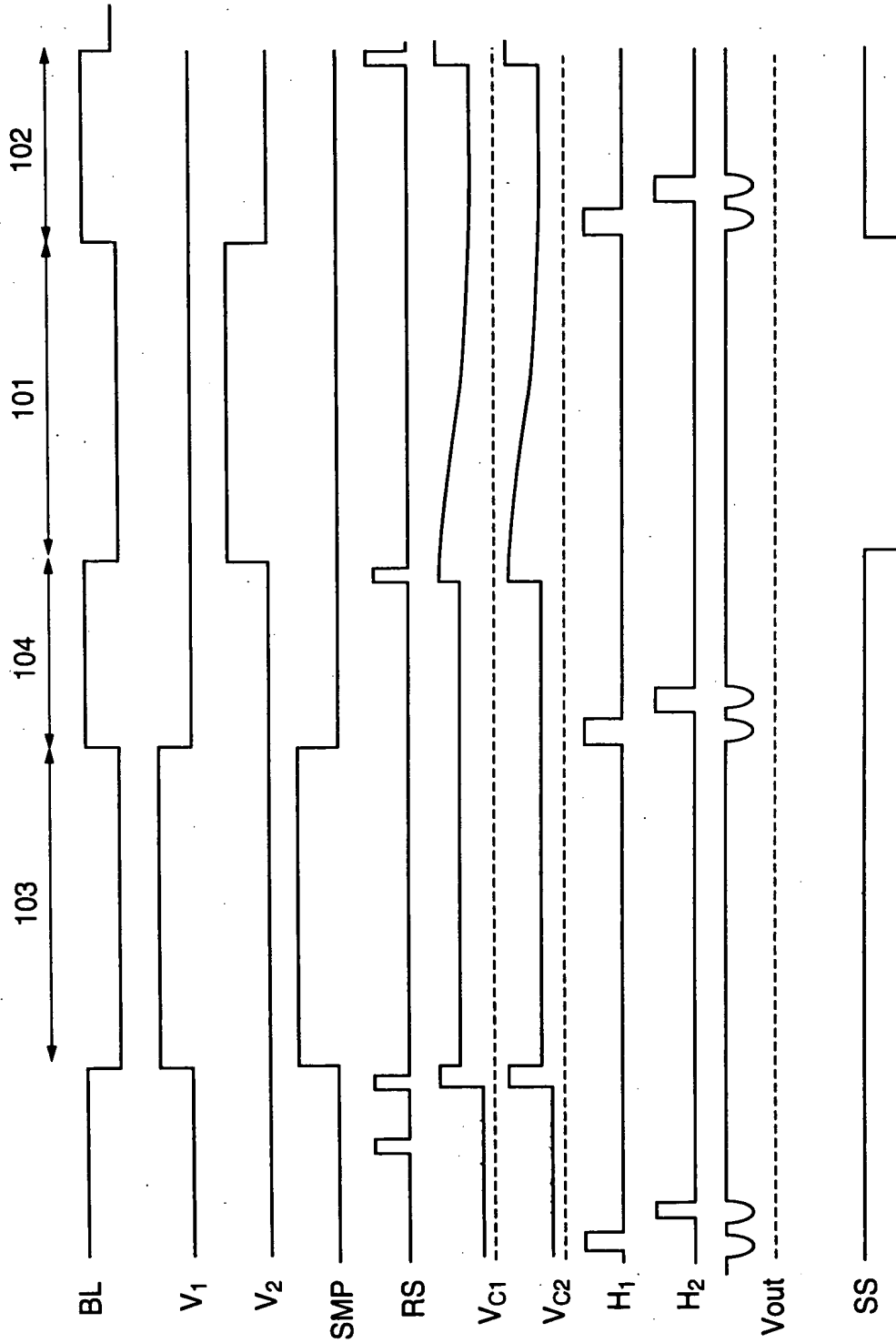
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FIG. 7



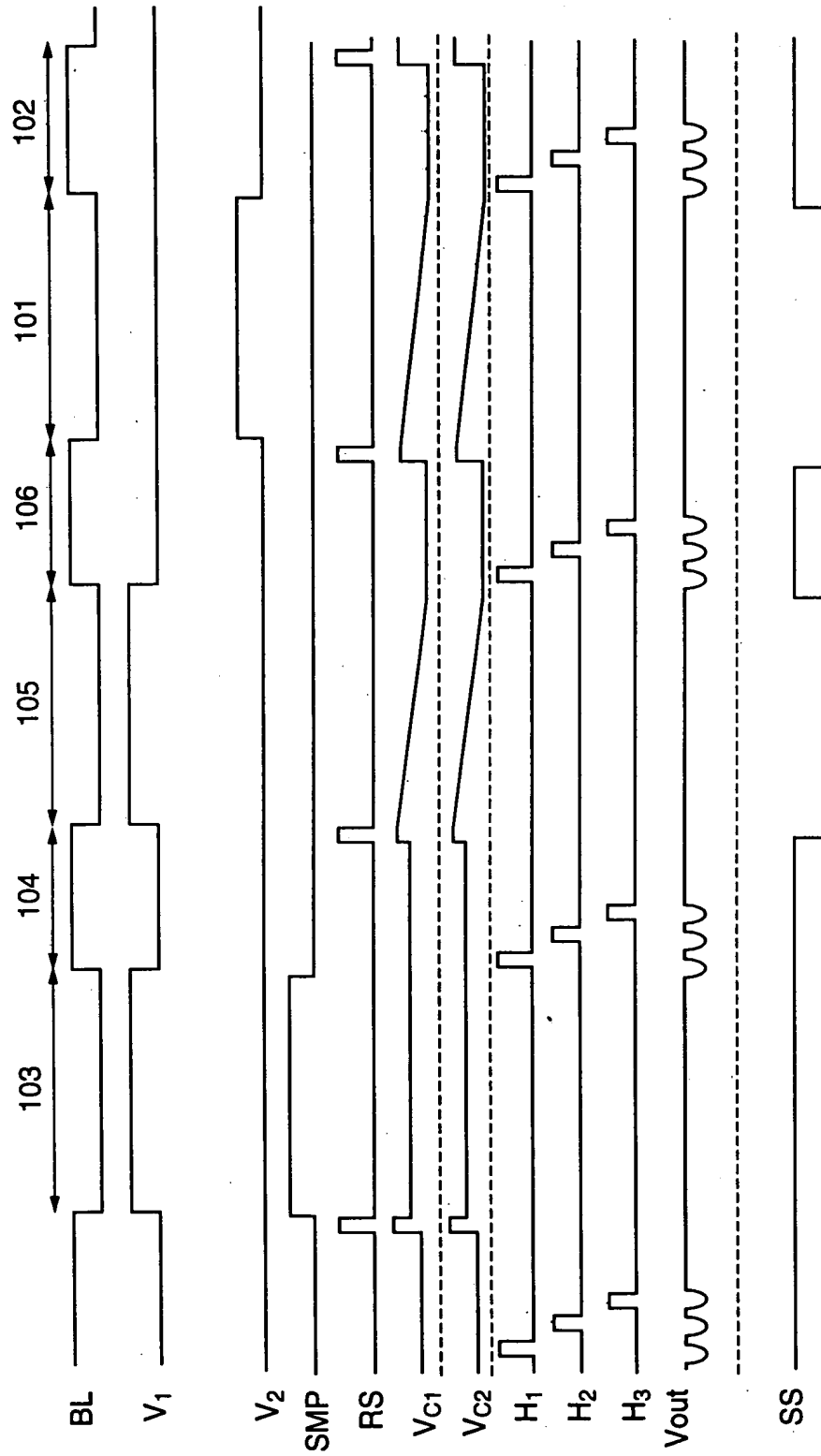
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FIG. 8



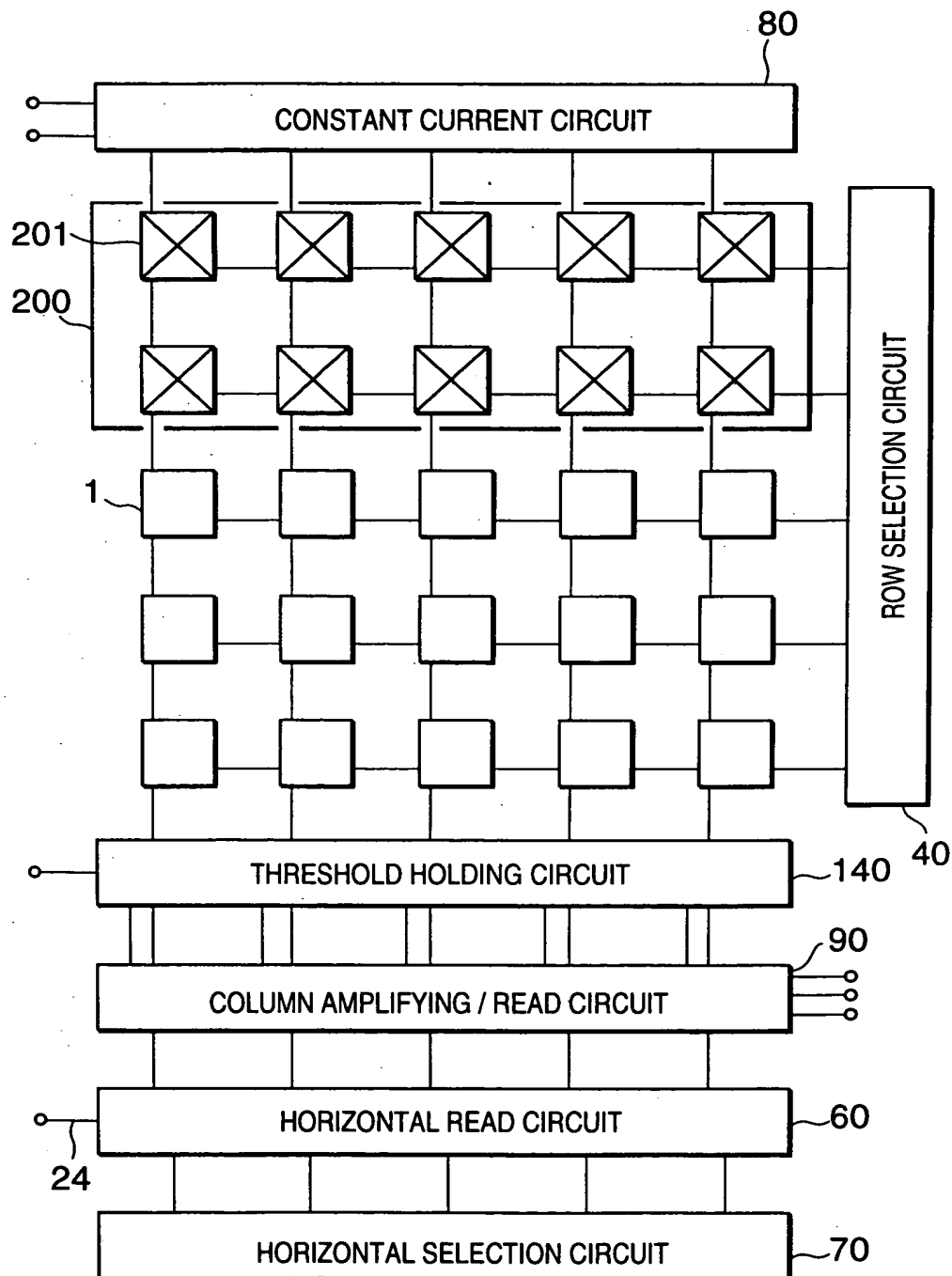
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FIG. 9



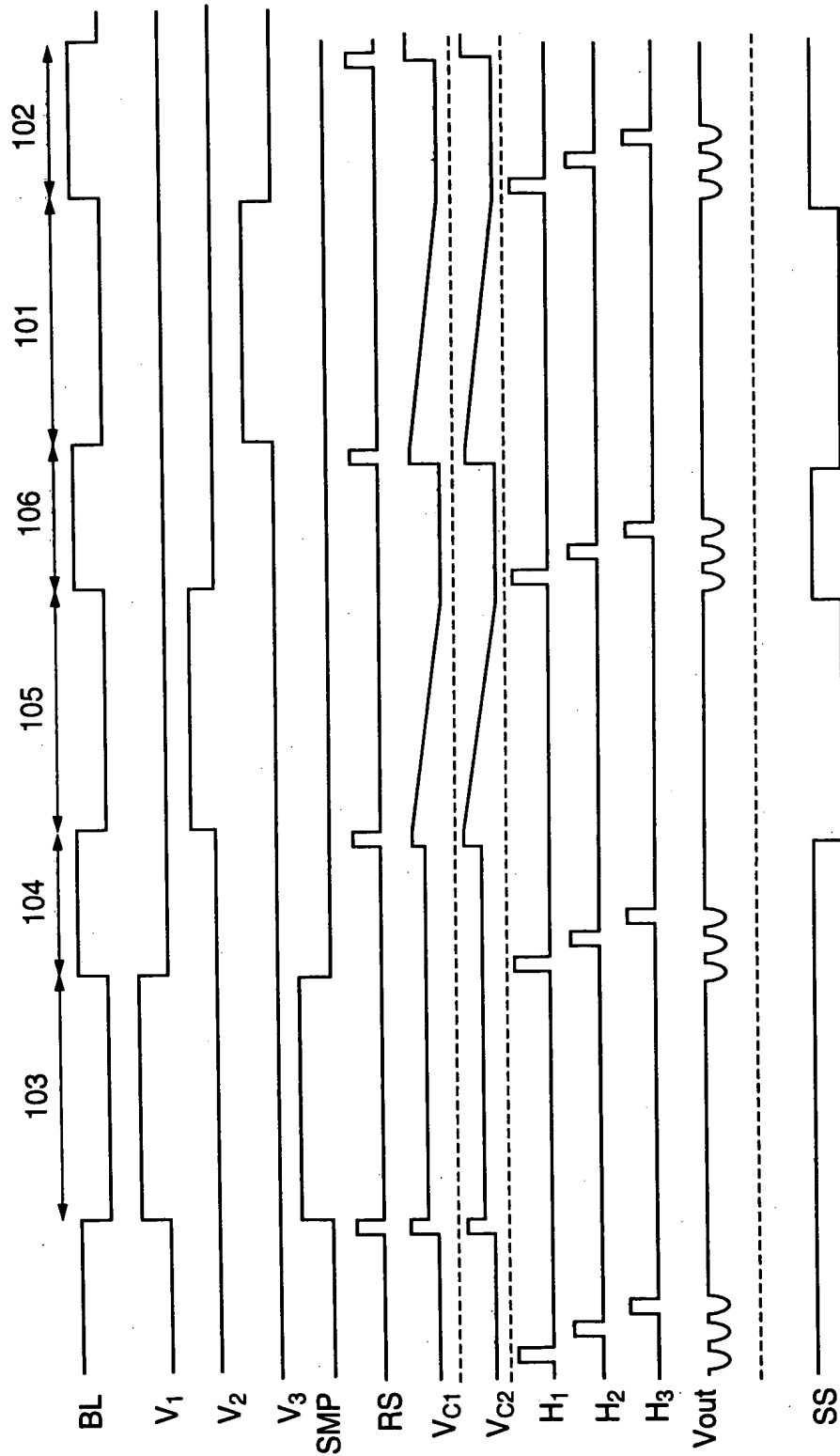
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FIG. 10



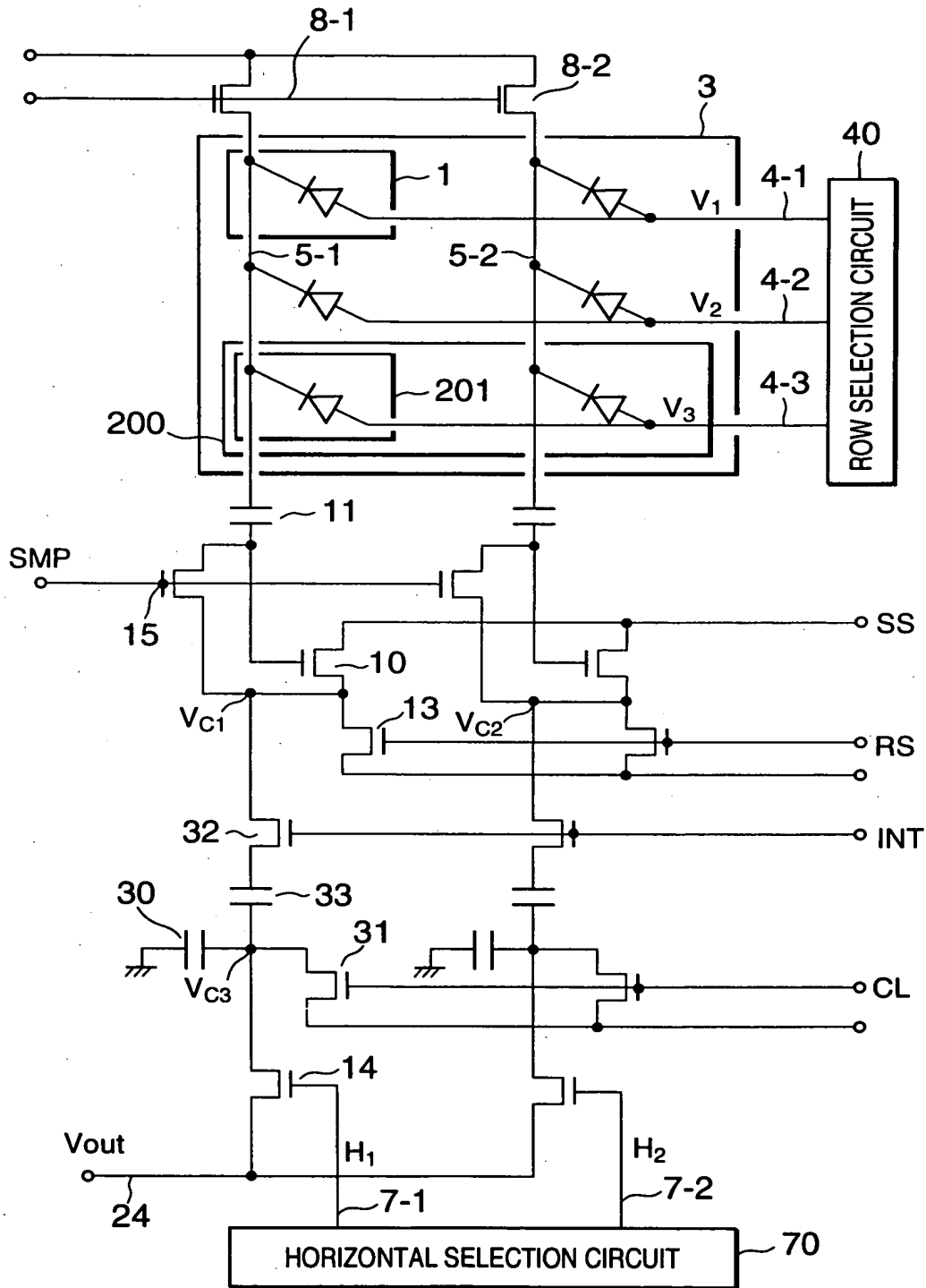
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FIG. 11



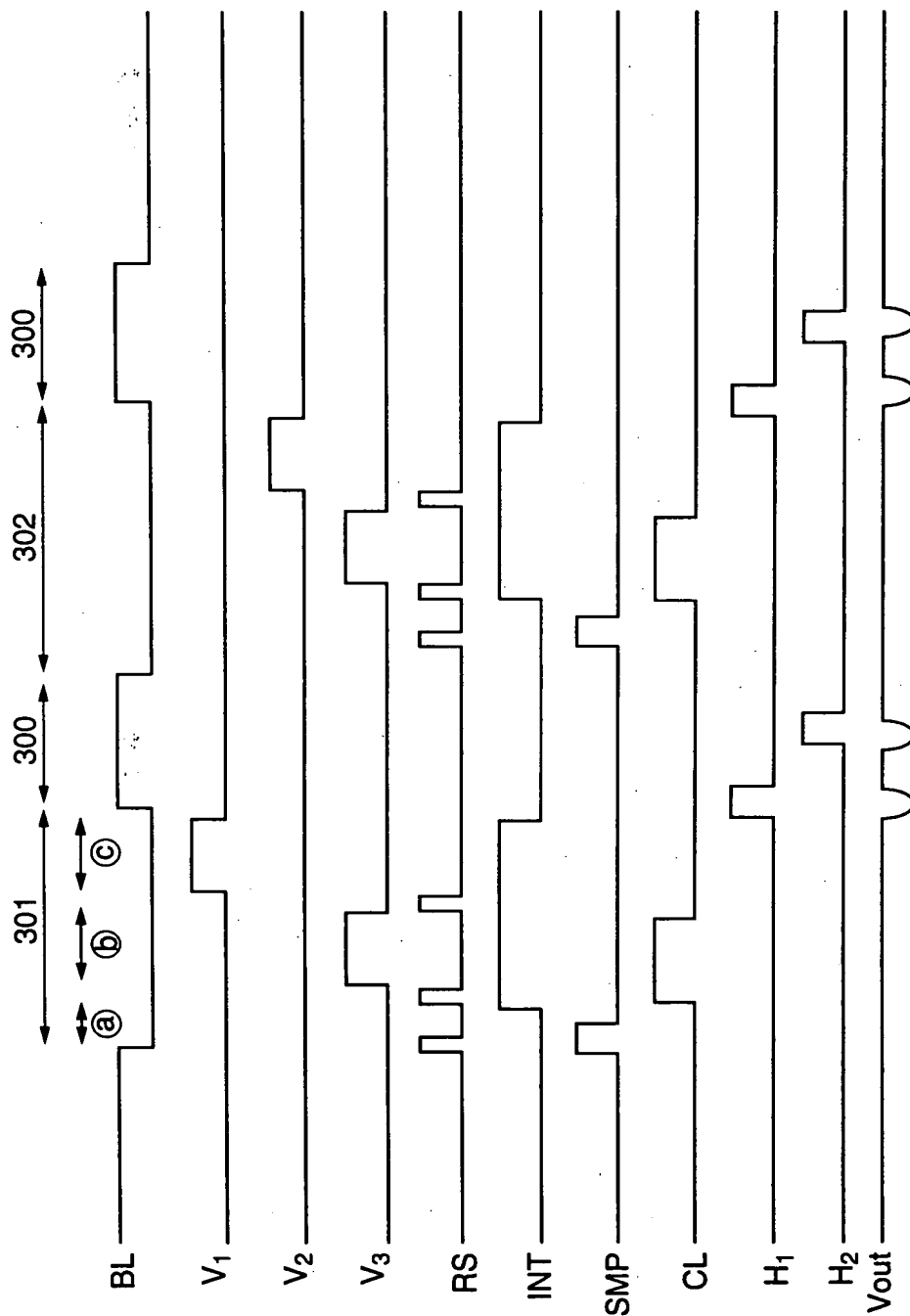
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FIG. 12



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FIG. 13



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FIG. 14

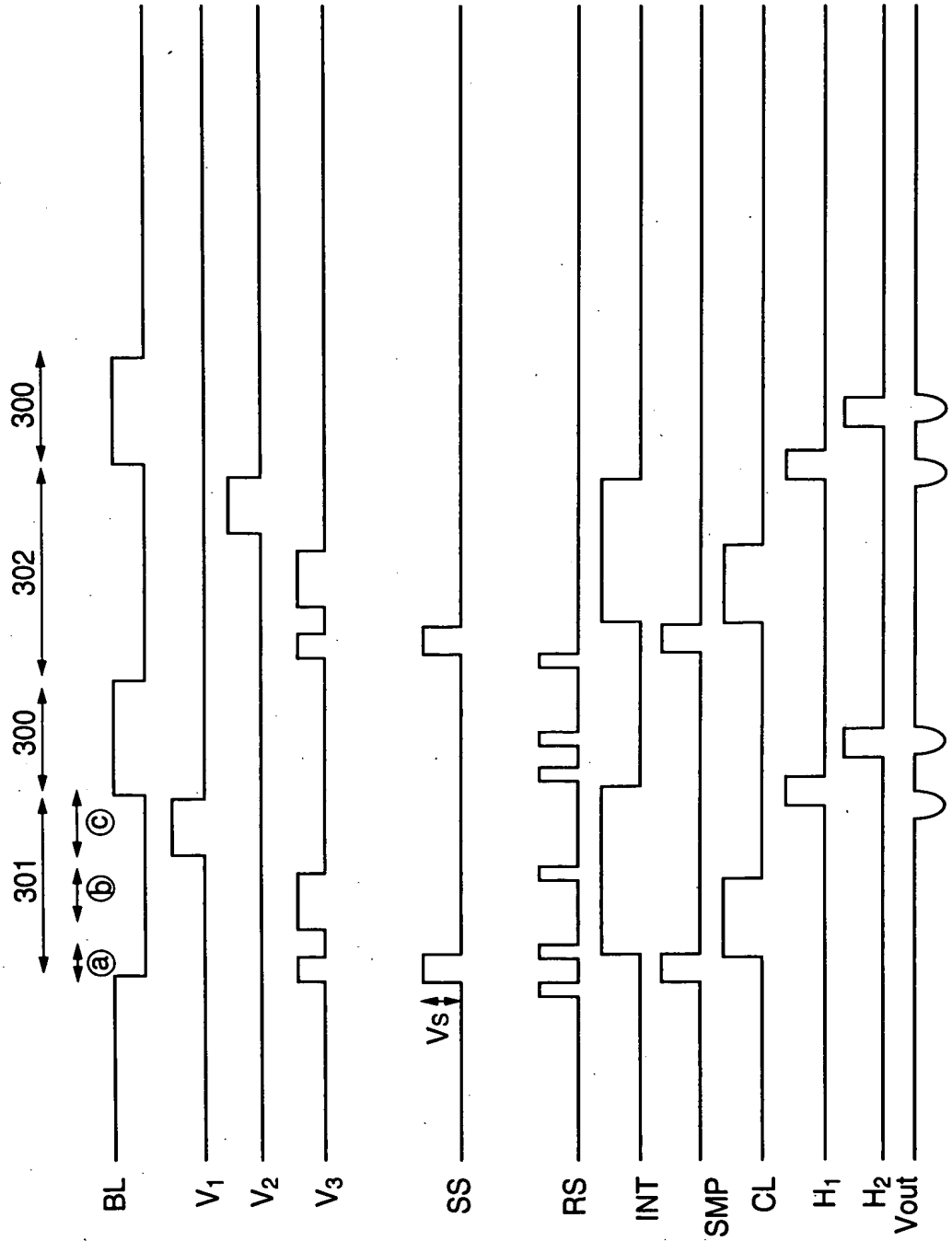
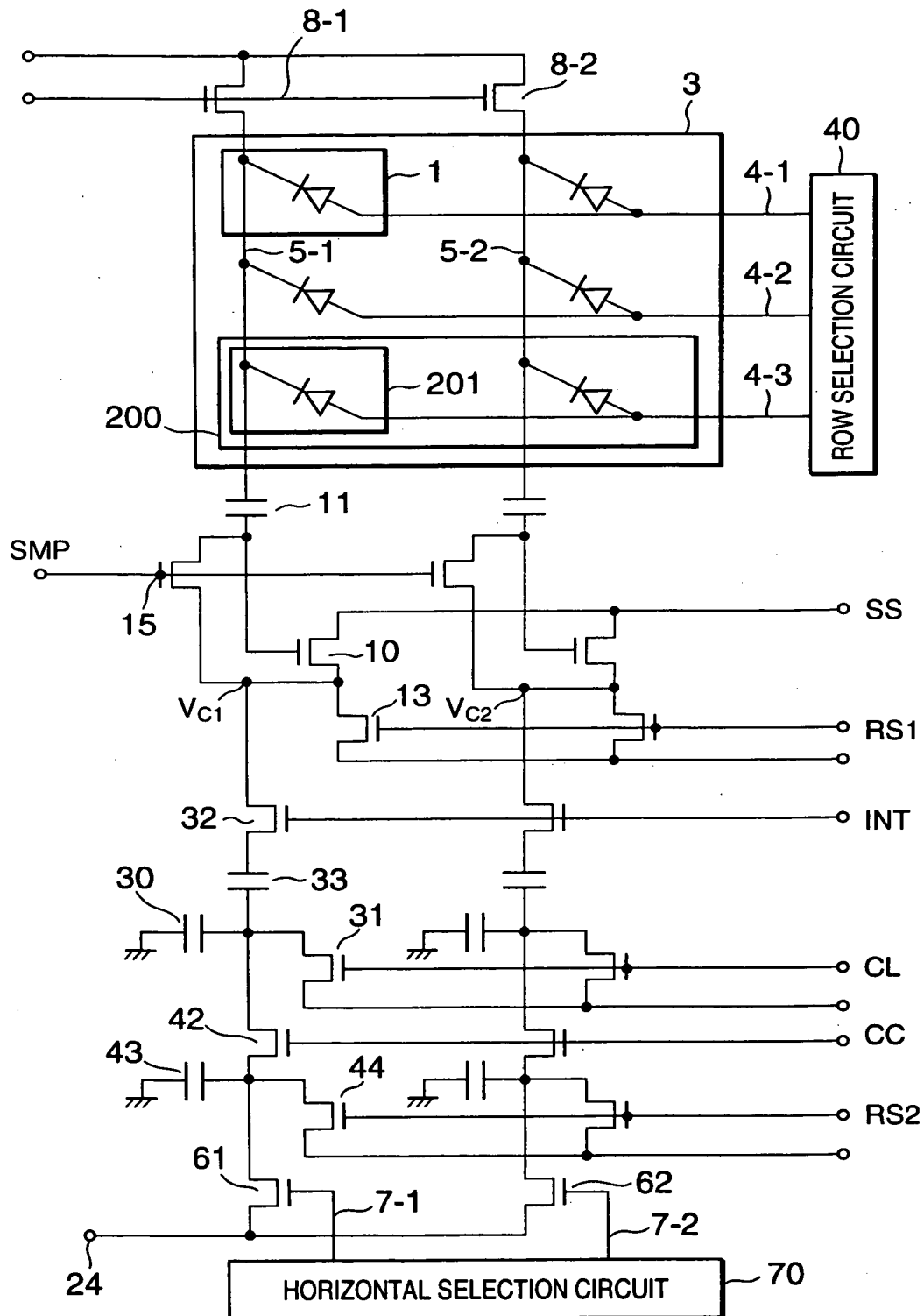
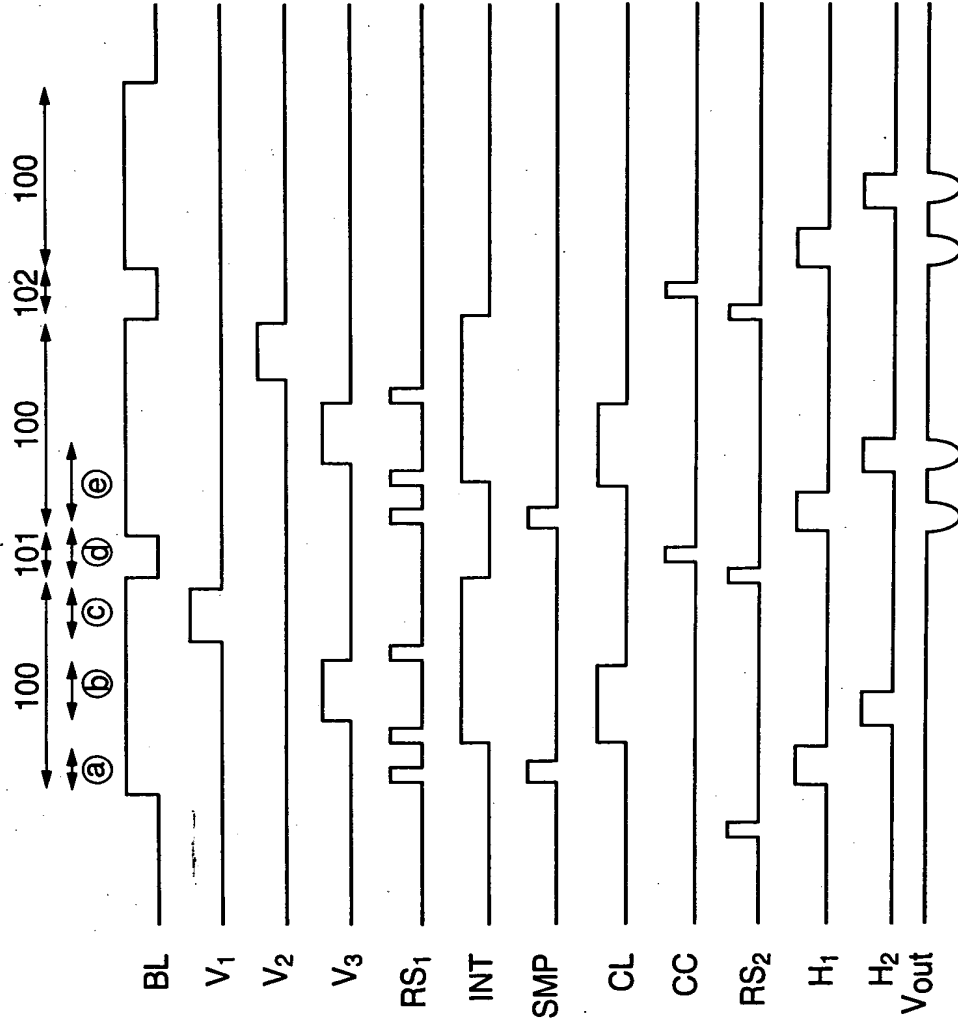


FIG. 15



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FIG. 16



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FIG. 17

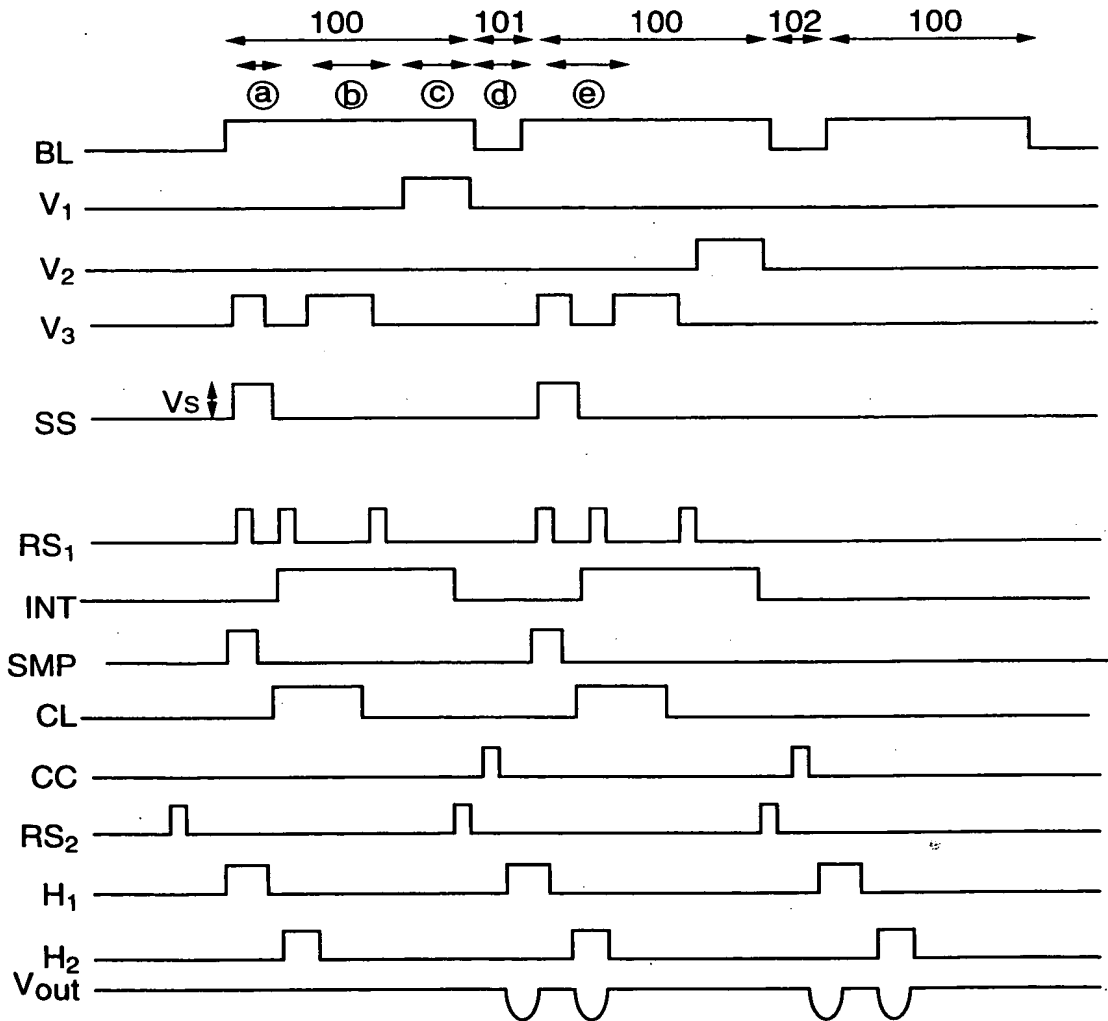
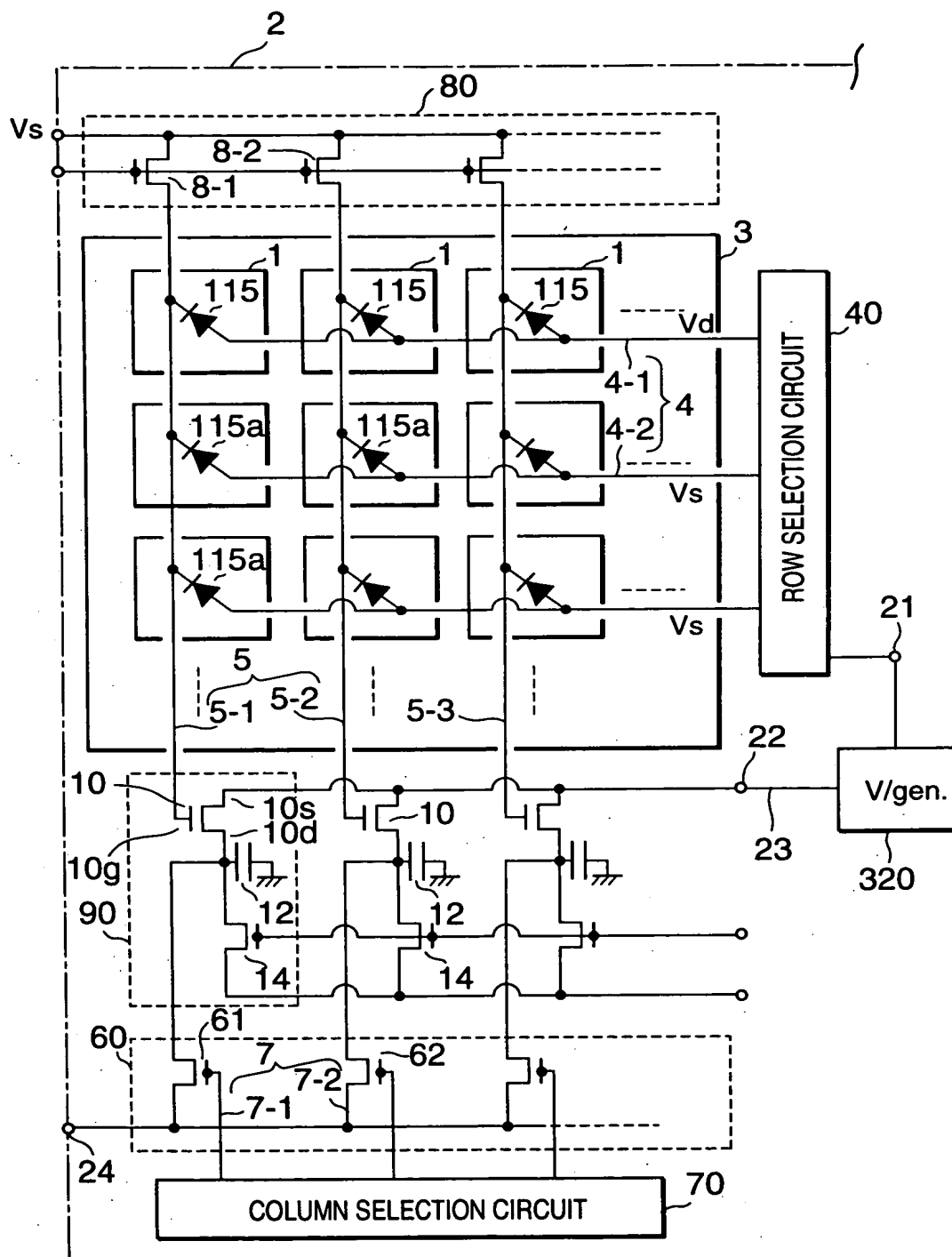


FIG. 18



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FIG. 19A

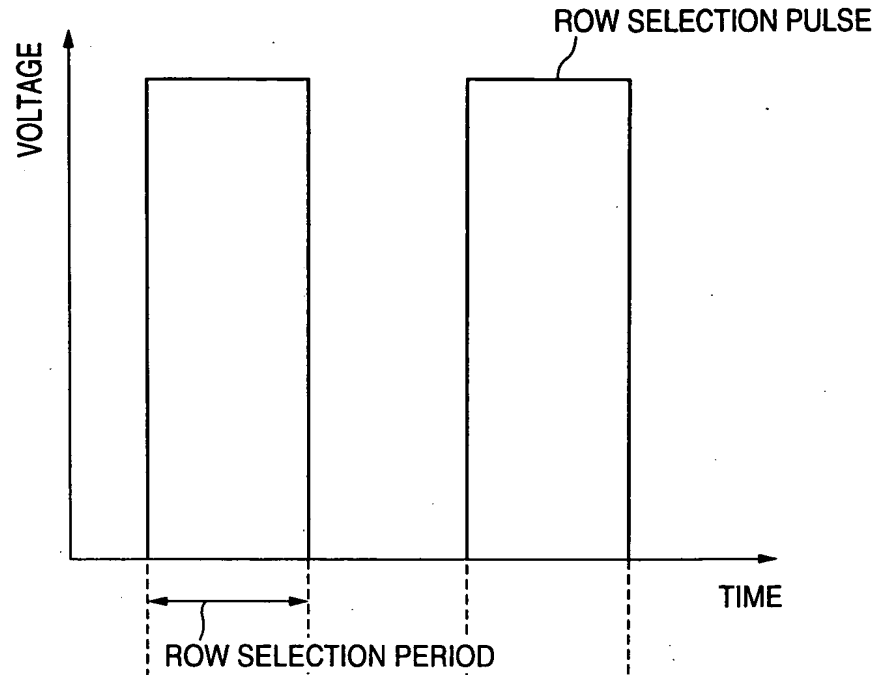
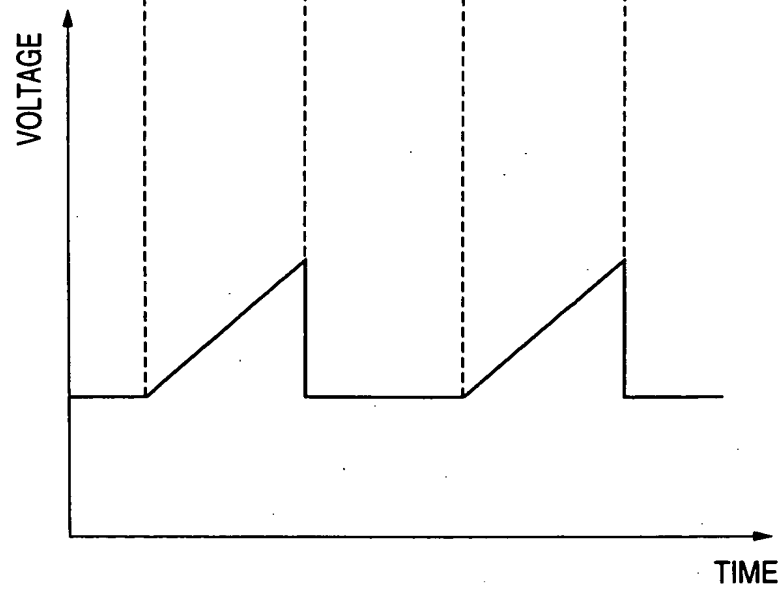


FIG. 19B



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FIG. 20A

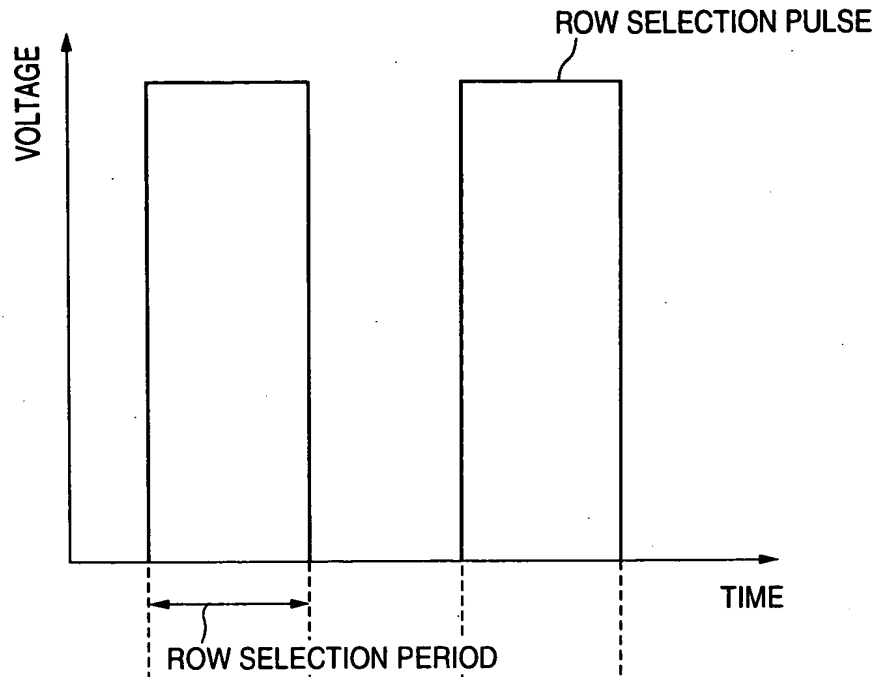
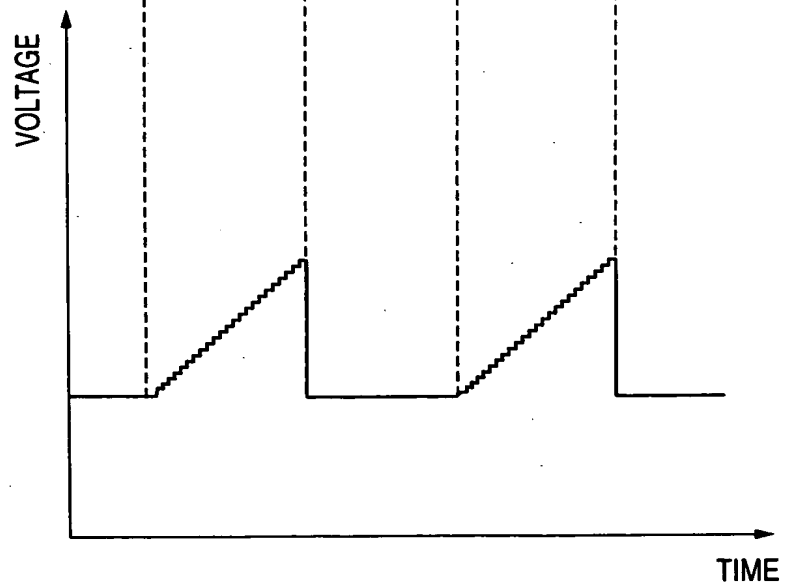
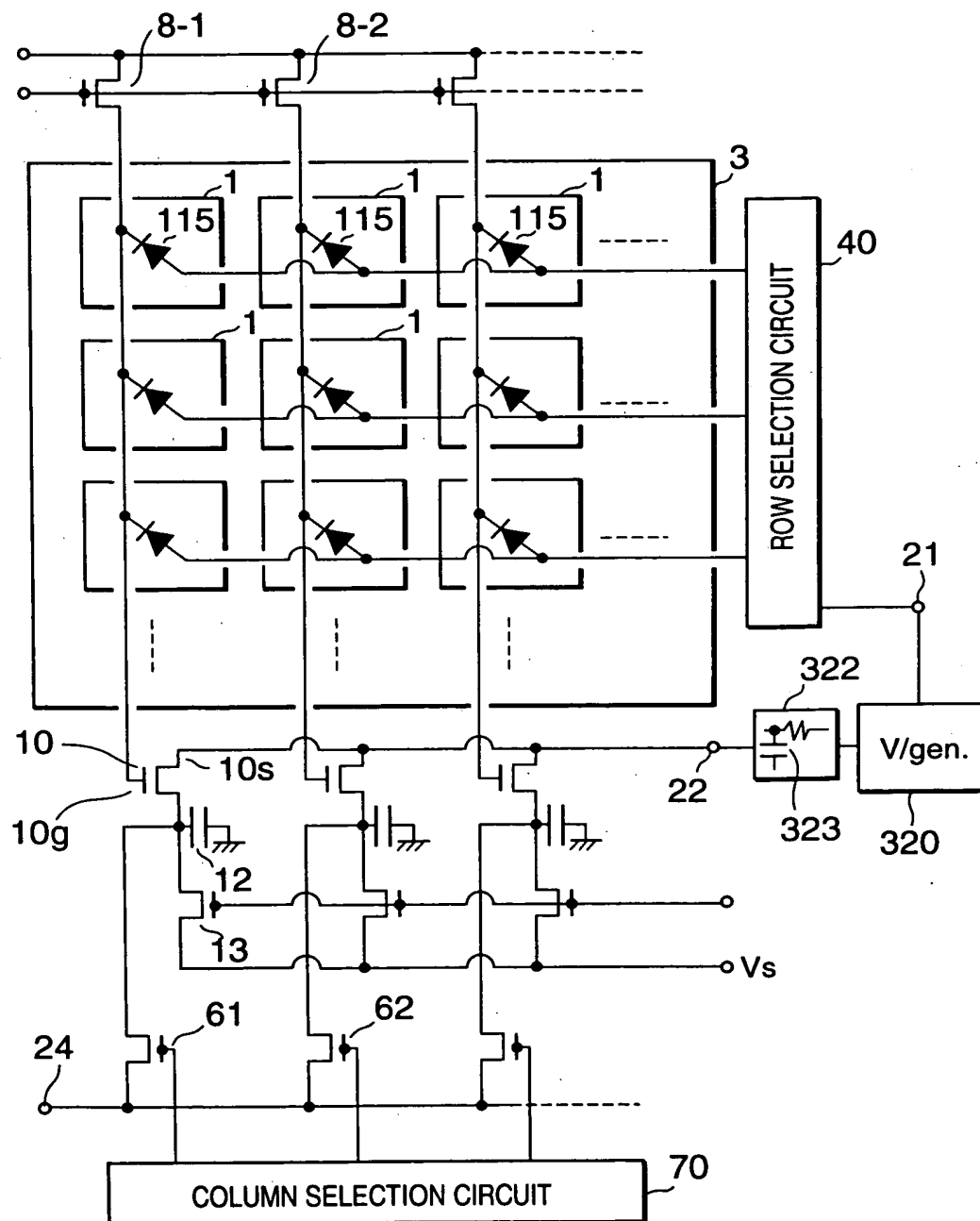


FIG. 20B



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FIG. 21



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FIG. 22A

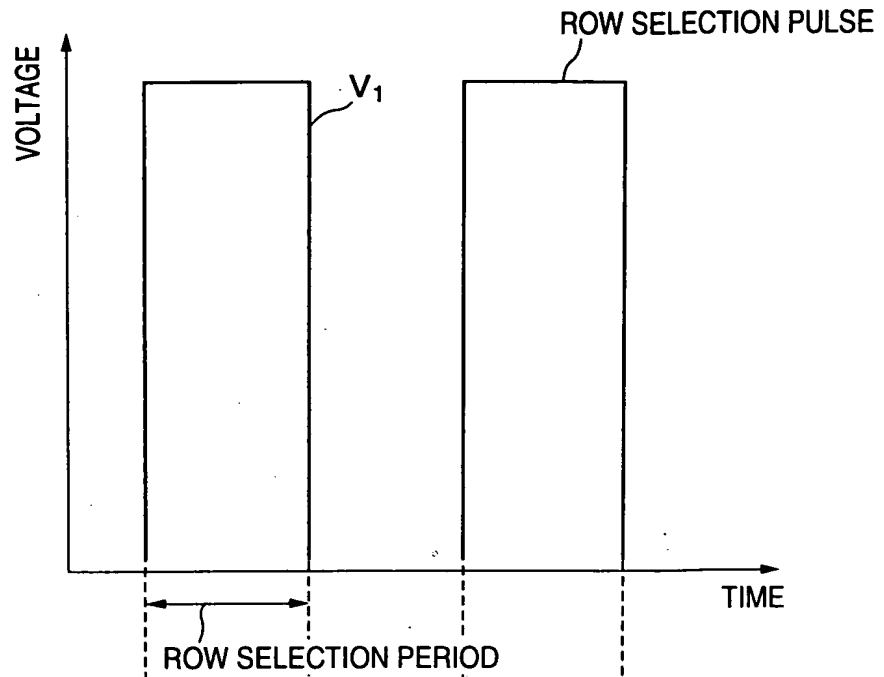
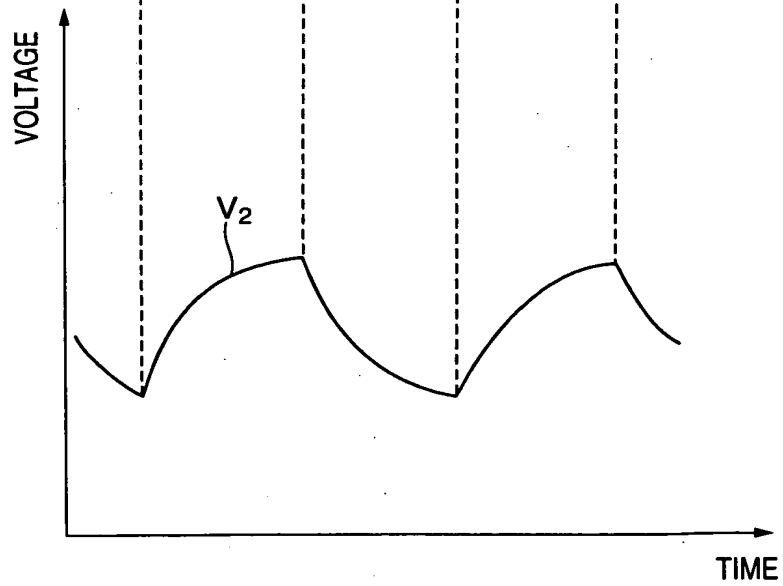
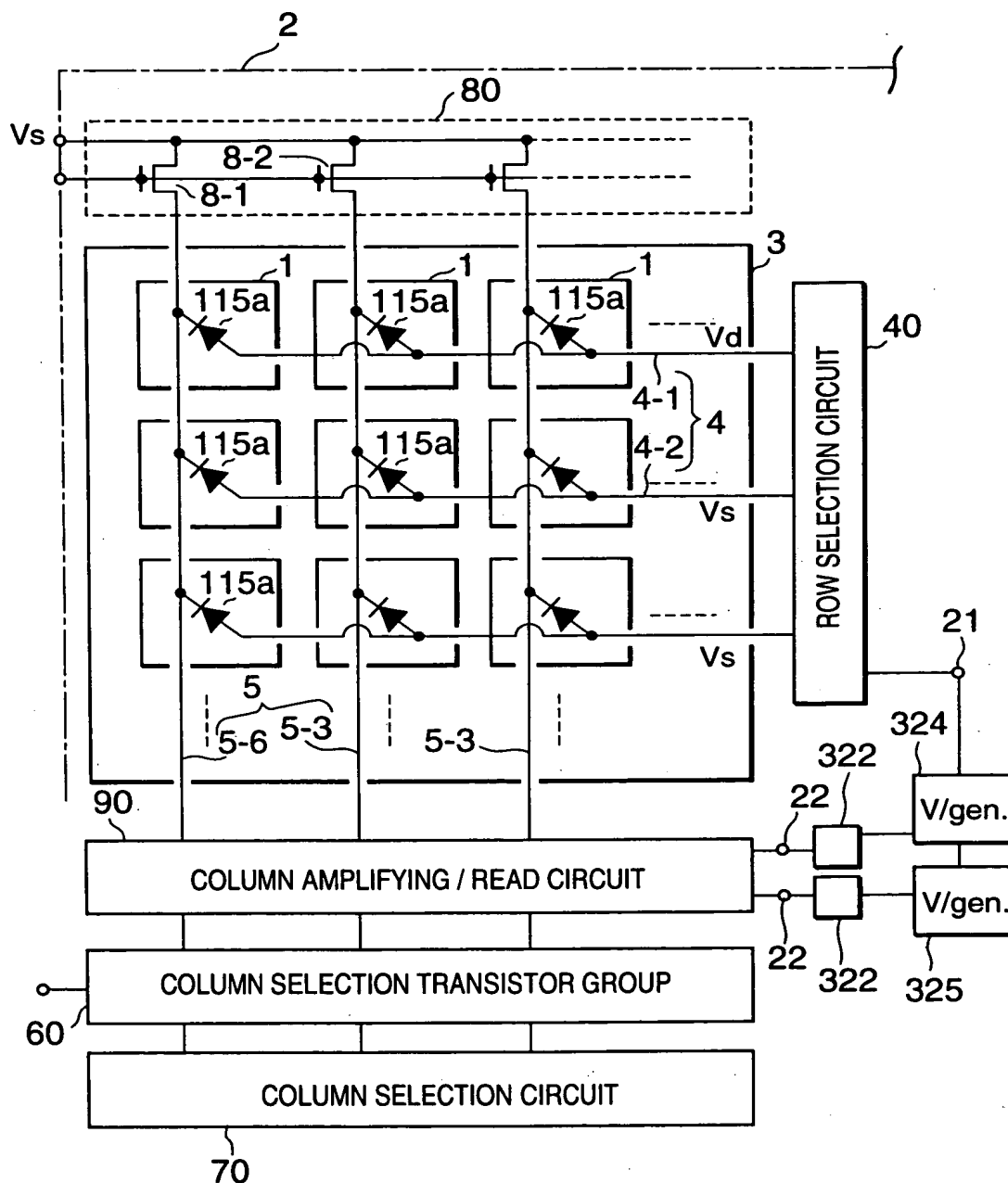


FIG. 22B



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FIG. 23



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FIG. 24A

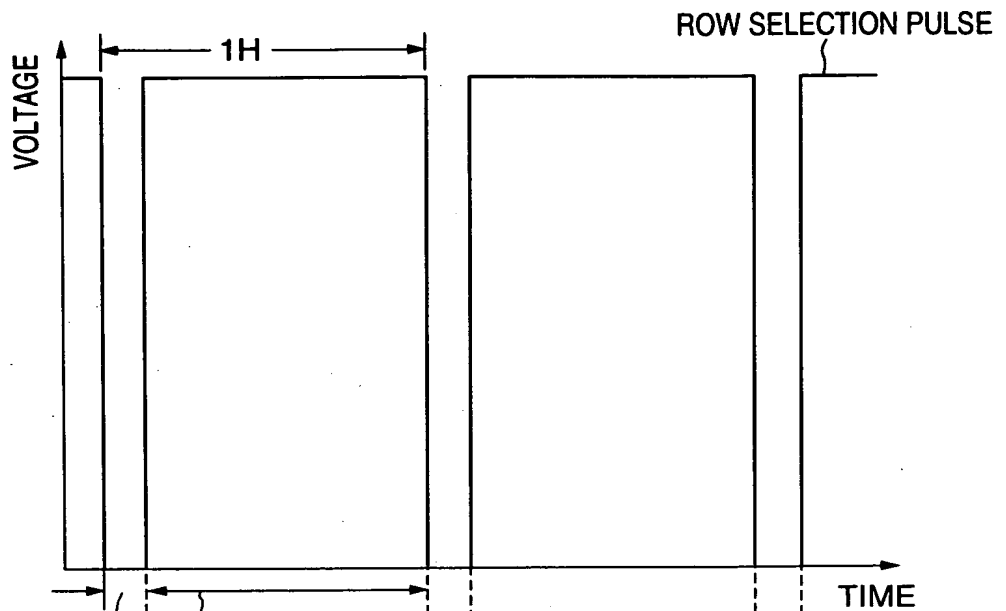


FIG. 24B

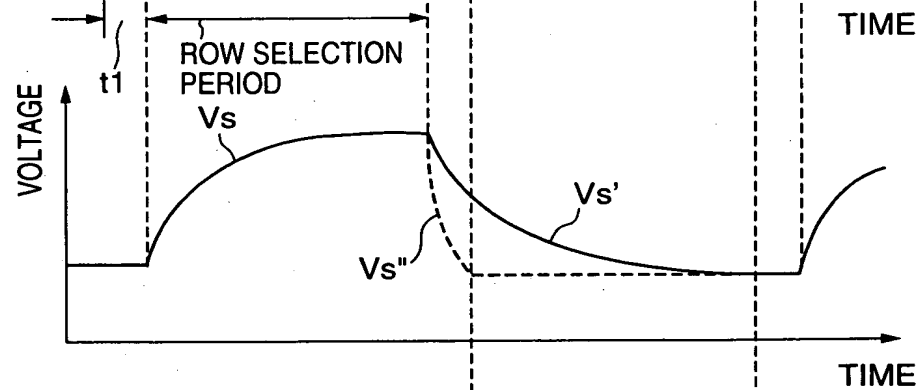
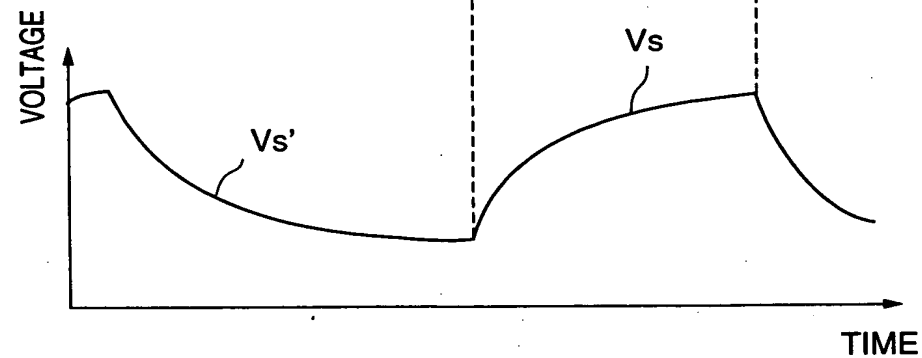
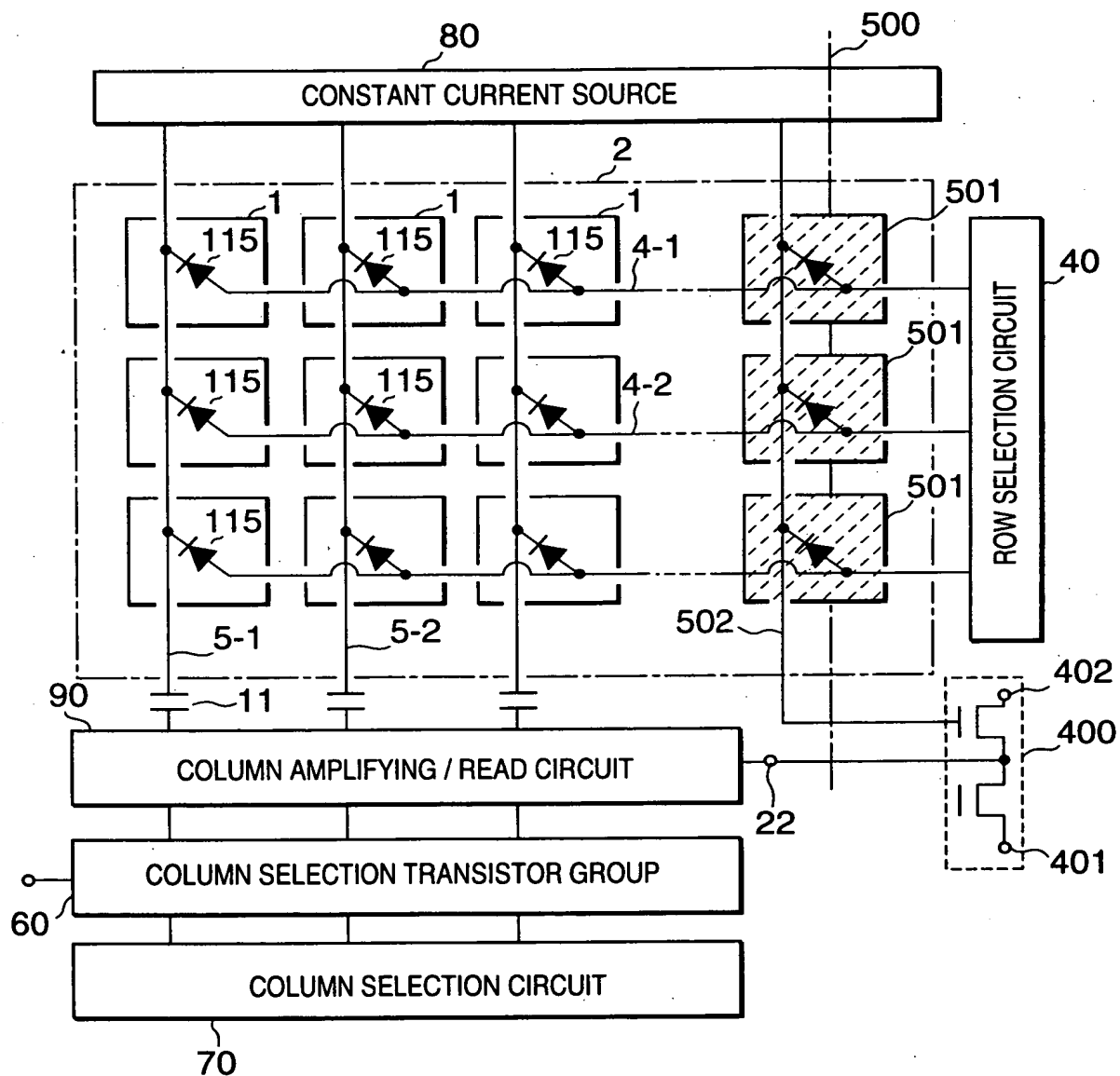


FIG. 24C



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FIG. 25



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FIG. 26

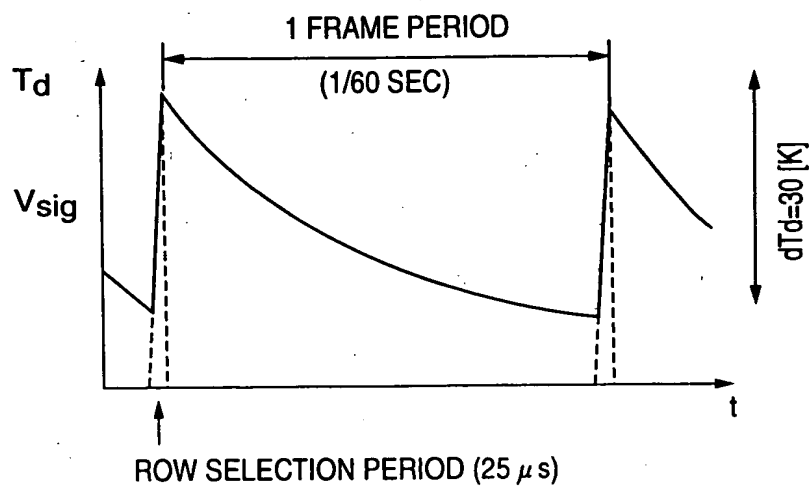


FIG. 27

